UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,510	03/26/2004	Fan Ho	24295/81401	1180

37803 7590 03/27/2007

SIDLEY AUSTIN BROWN & WOOD LLP
555 CALIFORNIA STREET
SUITE 2000
SAN FRANCISCO, CA 94104-1715

EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,510	HO, FAN	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *21-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I (claims 1-20) in the reply filed on 06/09/2006 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-12 and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kledzik (US 5,266,912).

4. Regarding claim 1, Kledzik (e.g. figs. 1-3) A multi-chip module (MCM) comprising: a first integrated circuit (IC) chip 13 on a substrate 17/51; a first ground plane 33 coupled to the first IC chip; a second IC chip 17 on the substrate17/52; and a second ground plane 21/33 coupled to the second IC chip.

5. Regarding claim 2, Kledzik shows that the first and second ground planes is coupled to at least one external lead 27 of the MCM.

6. Regarding claim 3, Kledzik shows that the at the first and second ground planes is is formed as respective trace on the substrate.

7. Regarding claim 4, Kledzik shows that the at the first and second ground planes is substantially rigid (col. 2/lls. 36-59). Note that substrate retains it shape at normal condition.

8. Regarding claim 5, Kledzik shows that the at the first and second ground planes is substantially flexible (col. 2/lls. 36-59). Note that the layer comprises a cu layers formed on a polyimide layer. This type of structure can be considered flexible since both of the layers exhibit some degree of flexibility.

9. Regarding claim 6, Kledzik shows that the first and second planes are comprise a strip of conductive material (col. 2/lls. 36-59).

10. Regarding claim 7, Kledzik shows that the first and second planes are comprise a layer of conductive material (col. 2/lls. 36-59).

11. Regarding claim 8, Kledzik shows that the first and second planes comprise a substantially solid layer of conductive material (col. 2/lls. 36-59).

12. Regarding claim 9, Kledzik teaches that the first and second ground planes comprise a grid of conductive material. Note that the ground plane is part of a ping grid array.

13. Regarding claims 10 and 11, Kledzik shows that the first chip is bonded/attached to the first ground plane, and the second chip is bonded/attached to the second ground plane. Note that the chips are connected to the upper layers that are bonded/attached to the ground planes.

14. Regarding claims 12 and 14, Kledzik shows that the first and second chips comprise DRAMS (col. 1/lls. 15-27).

15. Regarding claim 15, Kledzik shows that the first and second chips are application specific integrated circuits (e.g. ROM, SRAM, DRAM; col. 1/lls. 15-27).

16. Regarding claim 16, Kledzik shows one of the first and second chips is coupled to a plurality of input/output connectors 27 of the MCM and the other of the first and second chips is not coupled to any input/output connectors of the MCM. In this case, the chips of the package 53 can be recognized as the second chip.

17. Regarding claim 17, Kledzik shows that the first chip is coped to the second chip via at least one trace 43.

18. Regarding claims 18 and 19, Kledzik shows that at least one of the first and second chips may be tested without affecting operation of the other of the first and second chips in the MCM. Note that packages are independent units. Therefore, they can be independently tested.

19. Regarding claim 20, Kledzik first power plane coupled to the first IC chip; and a second power plane couple to the second IC chip (col. 7/lls. 15-25).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kledzik (US 5,266,912) in view of Wolf.

22. Kledzik shows most aspects of the instant invention including chips attached to the first and second ground planes. However, Kledzik does not disclose that solder balls (flip chip technique) can be used as connection means. Nonetheless, the use of

solder balls as connection means is considered an obvious design choice and it is not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416. For example, the advantages of flip chip bonding (solder ball or C4) are: 1) the entire chip surface can be covered with solder bumps. In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter interconnections on a die with the same size, and 2) the very short lengths of the chip to package interconnection paths minimizes their inductance (see Wolf pages 857-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder balls to make the electrical connections of the device disclosed by Kledzik in order to provide more I/O capability and to minimizes the inductance as taught Wolf.

Response to Arguments

23. Applicant's arguments filed 12/29/2006 have been fully considered but they are not persuasive. Applicant argues that Kledzik does not disclose a second ground. As shown in figure 3, is a schematic depicture of a stack of packages 51-53. Although not labeled the substrate 53-51 include the basic limitation of package 21 thus the bottom layer of 53-51 correspond to the ground layer 33 depicted in figure 2. Kledzik teaches in col. 5/lls. 56-60, "*In some cases, additional layers of circuit traces 31, 32, and 33 may be incorporated into or below the substrate 17, in the configuration of a multilevel printed circuit board. In many cases, one layer, such as layer 33, is configured as a*

ground plane. In this manner, the module 11 can be constructed with a controlled electrical impedance, as determined by various factors". In this case, any layer connected to the layer 33 in the same substrate or in other substrate is recognized as ground plane because is connected to the ground.

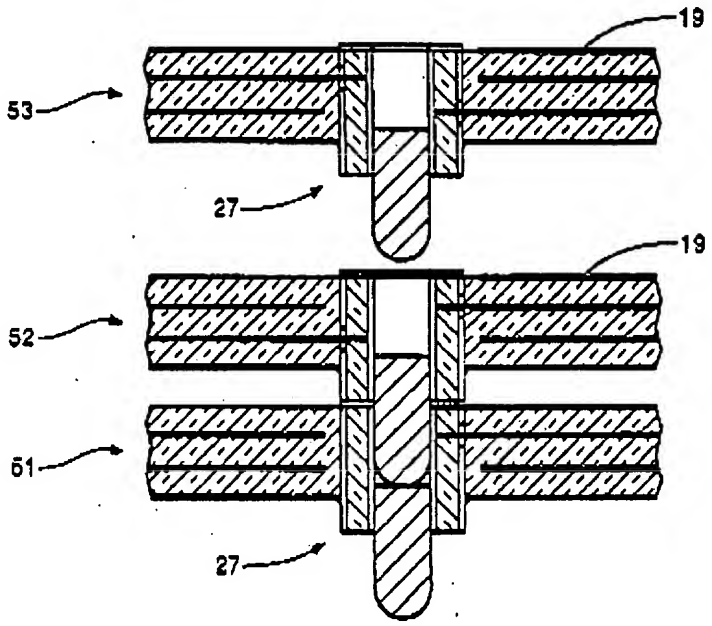

FIG. 3

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andujar
Primary Examiner
Art Unit 2826

08/17/2006